Lecture 24: Cache money & virtual memory

CMPE 120: Computer Organization & Architecture

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Logistics

- Reminder: check-in with professor is 1% of your final grade
  - Sign up link
- Grade remediation plan
  - 30+ students have already signed up
  - Slots are getting booked quickly → sign up soon!
- HW5 released last Thursday. Start now!

Grade remediation plan

- HW1 Quiz Remediation: meet with professor for 15 minutes
  - Bring a newly hand-written solution. Explain what you got wrong on your quiz and your new solution.
  - Replaces HW1 quiz grade & drops lowest HW Quiz grade
  - Schedule a time on my calendar in the next ~3 weeks (10/30 - 11/20)
    - Link: https://calendar.app.google/d3D4hm3JbmpXcrVt5
    - 100 appointment slots available for 67 students
    - If none of these times work, email me to schedule a time during this window.

- Final exam grade can replace the midterm grade if higher
  - → Midterm grade replacement = max(final exam grade, midterm exam grade)

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  - No rules on what data can go where

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- But, some new considerations:
  - Where do you look to find an element?

  - How to decide what to remove?

Fully associative cache

Item	Addr b10	Addr b2	H/M?
A[0]	16	00010 000	
B[0]	48	00110 000	
A[1]	20	00010 100	
B[1]	52	00110 100	
A[0]	16	00010 000	
B[0]	48	00110 000	
A[1]	20	00010 100	
B[1]	52	00110 100	

Each block holds 2 words (8 bytes)

tag	data

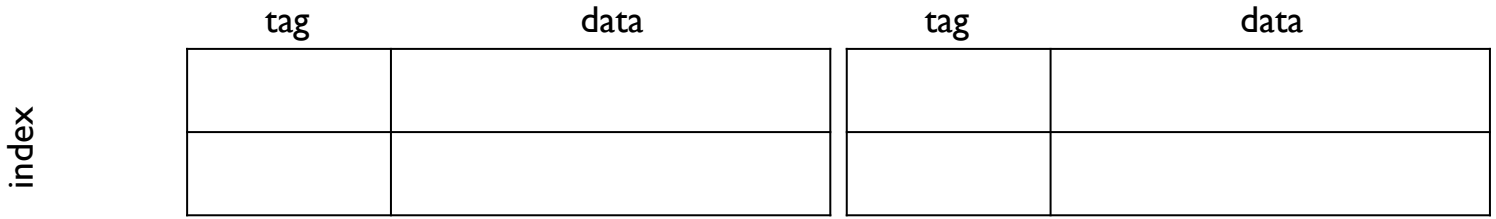
What is the hit rate on this cache?

A. 75%
B. 50%
C. 25%
D. 12.5%
E. 0%

Set associativity

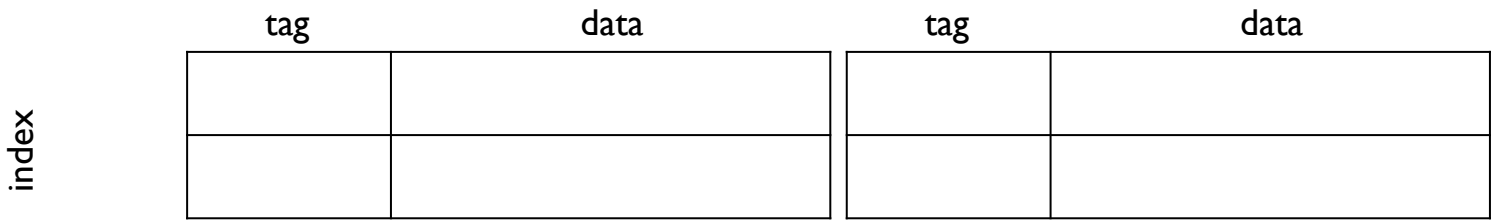
- n-way set-associative cache
  - Each index can store n blocks
  - All blocks sharing an index are in a set

- Example: 4 blocks
  - each block holds 2 words, 2 blocks per index



Set associativity

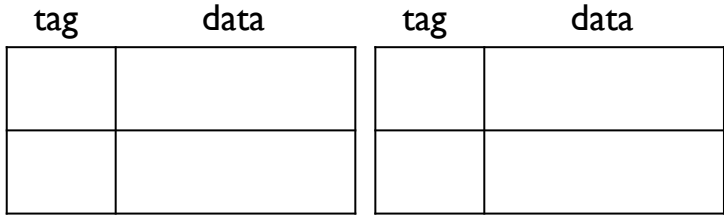
- Consider again:
  - Where do you look to find an element?
  - How to decide what to remove?



2-way set-associative cache

Each block holds 2 words (8 bytes)

Item	Addr b10	Addr b2	H/M?
A[0]	16	0001 0 000	
B[0]	48	0011 0 000	
A[1]	20	0001 0 100	
B[1]	52	0011 0 100	
A[0]	16	0001 0 000	
B[0]	48	0011 0 000	
A[1]	20	0001 0 100	
B[1]	52	0011 0 100	



What is the hit rate on this cache?

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C. 25%
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E. 0%

Set associative caches

- Performance is middle-ground between directed mapped & fully associative
  - Decent hit times
  - Decent use of cache space

- Hybrid design between direct mapped & fully associative

- Hit rates generally higher than direct mapped

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- To do LRU, must know true ordering of accesses
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- To do LRU, must know true ordering of accesses
  - Need extra bits to keep track of order
  - Ex: 4-way set-associative cache, each block has metadata on if accessed
    - 00: least recently
    - 01: second least recently
    - 10: second most recently
    - 11: most recently
  - All bits updated on every access (hit or miss)

Key caching formulas

- With n-way associative caches
  - `num_block_offset_bits = log2(block_size_in_bytes)`
  - `num_cache_entries = cache_size / (block_size * n)`
  - `num_index_bits = log2(num_cache_entries)`
  - `num_tag_bits = address_size - num_index_bits - num_block_offset_bits`

Summary: Cache miss types

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- Capacity miss: missed only because cache is not big enough
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Summary: Cache miss types

- Compulsory (or cold-start) miss: first access to data

- Capacity miss: missed only because cache is not big enough
  - Address has already been requested
  - AND fully-associative cache of same size would also experience miss

- Conflict miss: missed because of indexing
  - Address has already been requested
  - AND fully-associative cache of same size would also experience hit

Virtual memory

What if ISA has address space bigger than physical memory?

- 64-bit address space with byte addressability = 16 Exabytes

Remember processes?

With one RAM, how can we run multiple processes?

Memory virtualization

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- Memory virtualization: divide up physical RAM into smaller "virtual" memory spaces
  - So each process thinks it has its own memory
  - The physical memory can be smaller than the ISA's address space
  - Hardware and software cooperatively manage how virtual memory maps to physical memory

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- Address translation maps virtual address to a physical address