Lecture 24: Cache money & virtual memory

CMPE 120: Computer Organization & Architecture

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Logistics

- Reminder: check-in with professor is 1% of your final grade
  - Sign up link

- Grade remediation plan
  - ~~30+~~ 40 students have already signed up
  - Slots are getting booked quickly → sign up soon!

6 slots left

- HW5 released last Thursday. Start now!

Grade remediation plan

- HW1 Quiz Remediation: meet with professor for 15 minutes
  - Bring a newly hand-written solution. Explain what you got wrong on your quiz and your new solution.
  - Replaces HW1 quiz grade & drops lowest HW Quiz grade
  - Schedule a time on my calendar in the next ~3 weeks (10/30 - 11/20)
    - Link: https://calendar.app.google/d3D4hm3JbmpXcrVt5
    - 100 appointment slots available for 67 students
    - If none of these times work, email me to schedule a time during this window.

- Final exam grade can replace the midterm grade if higher
  - → Midterm grade replacement = max(final exam grade, midterm exam grade)

Fully associative cache

- Fully associative cache: block can be placed in any cache location
  - No rules on what data can go where

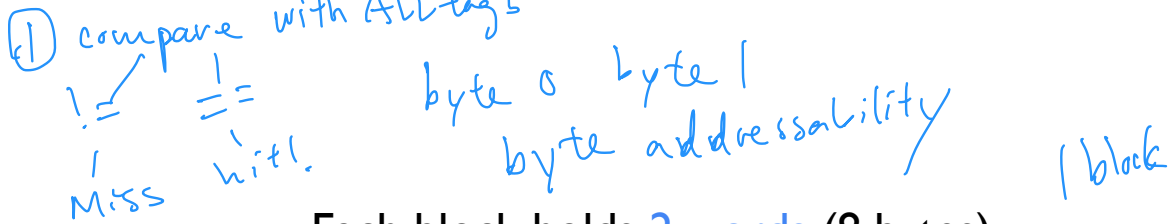
Fully associative cache

- Fully associative cache: block can be placed in any cache location
  - No rules on what data can go where

- But, some new considerations:
  - Where do you look to find an element?

  - How to decide what to remove?

Fully associative cache



Item	Addr b10	Addr b2	H/M?
A[0]	16	00010 000	M
B[0]	48	00110 000	M
A[1]	20	00010 100	H
B[1]	52	00110 100	H
A[0]	16	00010 000	H
B[0]	48	00110 000	H
A[1]	20	00010 100	H
B[1]	52	00110 100	H

tag

block offset

index for a byte in the block

Each block holds 2 words (8 bytes)

tag	0	1	2	3	data 4	5	6	7
00010					A[0]	A[1]		
00110					B[0]	B[1]		

block offset

What is the hit rate on this cache?

A. 75%
B. 50%
C. 25%
D. 12.5%
E. 0%

hits / # accesses

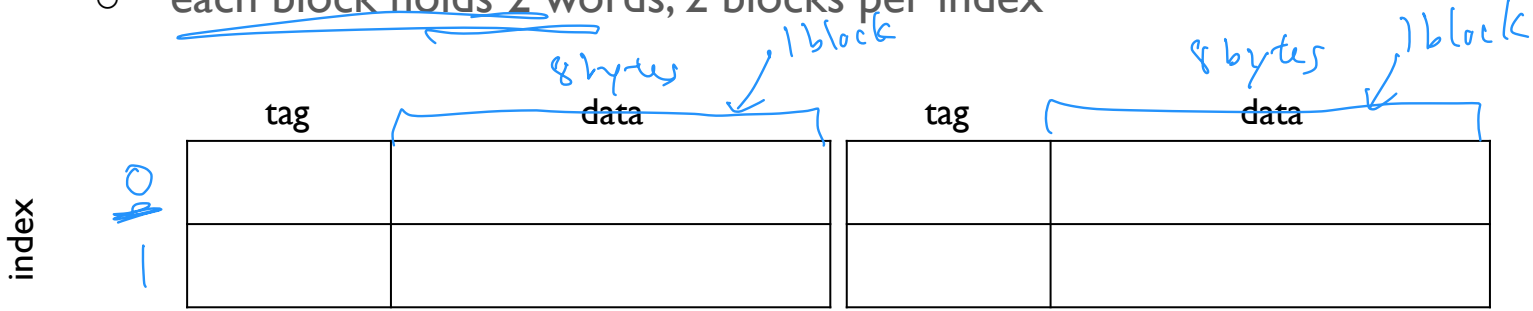
4 hits / 8 accesses

Set associativity

- n-way set-associative cache
  - Each index can store n blocks
  - All blocks sharing an index are in a set

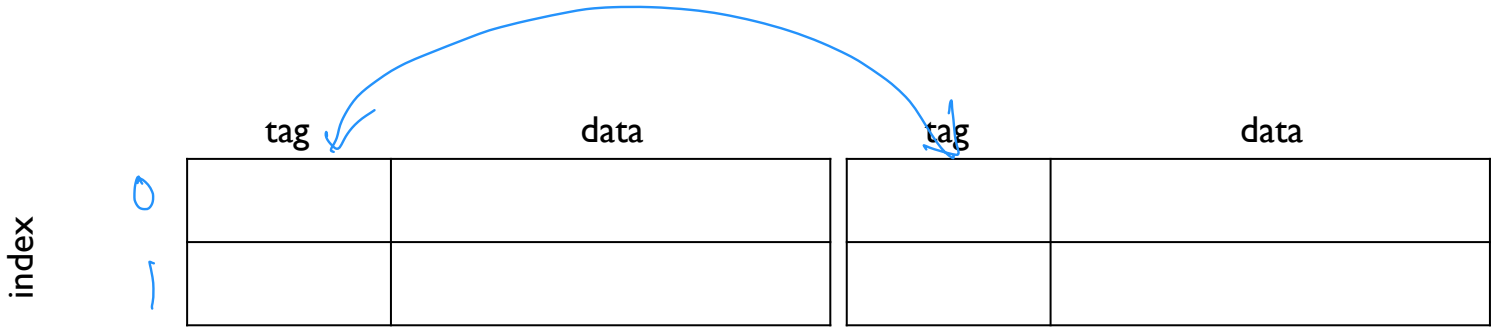
- Example: 4 blocks
  - each block holds 2 words, 2 blocks per index

2-way set associative cache



Set associativity

- Consider again:
  - Where do you look to find an element?
  - How to decide what to remove?



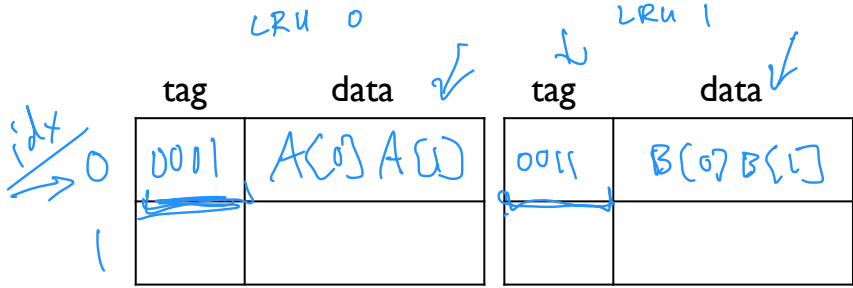
2-way set-associative cache

1. check index
2. compare tags in this set ONLY

Each block holds 2 words (8 bytes)

Item	Addr b10	Addr b2	H/M?
A[0]	16	0001 0 000	M
B[0]	48	0011 0 000	M
A[1]	20	0001 0 100	H
B[1]	52	0011 0 100	H
A[0]	16	0001 0 000	H
B[0]	48	0011 0 000	H
A[1]	20	0001 0 100	H
B[1]	52	0011 0 100	H

tag | idx bits | block offset bits



What is the hit rate on this cache?

A. 75%
B. 50%
C. 25%
D. 12.5%
E. 0%

Set associative caches

index & compare 1 tag

No indx compare ALL tags

- Performance is middle-ground between directed mapped & fully associative
  - Decent hit times
  - Decent use of cache space

- Hybrid design between direct mapped & fully associative
  - ↳ index & compare against tags in your set ONLY

- Hit rates generally higher than direct mapped

Least recently used (LRU)

- To do LRU, must know true ordering of accesses
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- To do LRU, must know true ordering of accesses
  - Need extra bits to keep track of order
  - Ex: 4-way set-associative cache, each block has metadata on if accessed
    - 00: least recently
    - 01: second least recently
    - 10: second most recently
    - 11: most recently
  - All bits updated on every access (hit or miss)

Key caching formulas

- With n-way associative caches
  - `num_block_offset_bits = log2(block_size_in_bytes)`
  - `num_cache_entries = cache_size / (block_size * n)`
  - `num_index_bits = log2(num_cache_entries)`
  - `num_tag_bits = address_size - num_index_bits - num_block_offset_bits`

Summary: Cache miss types

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- Capacity miss: missed only because cache is not big enough
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Summary: Cache miss types

- Compulsory (or cold-start) miss: first access to data

- Capacity miss: missed only because cache is not big enough
  - Address has already been requested
  - AND fully-associative cache of same size would also experience miss

- Conflict miss: missed because of indexing
  - Address has already been requested
  - AND fully-associative cache of same size would also experience hit

Virtual memory

What if ISA has address space bigger than physical memory?

- 64-bit address space with byte addressability = 16 Exabytes

2^{10} = 1 KB

2^{20} = 1 MB

2^{30} = 1 GB

2^{40} = 1 TB

2^{50} = 1 PB

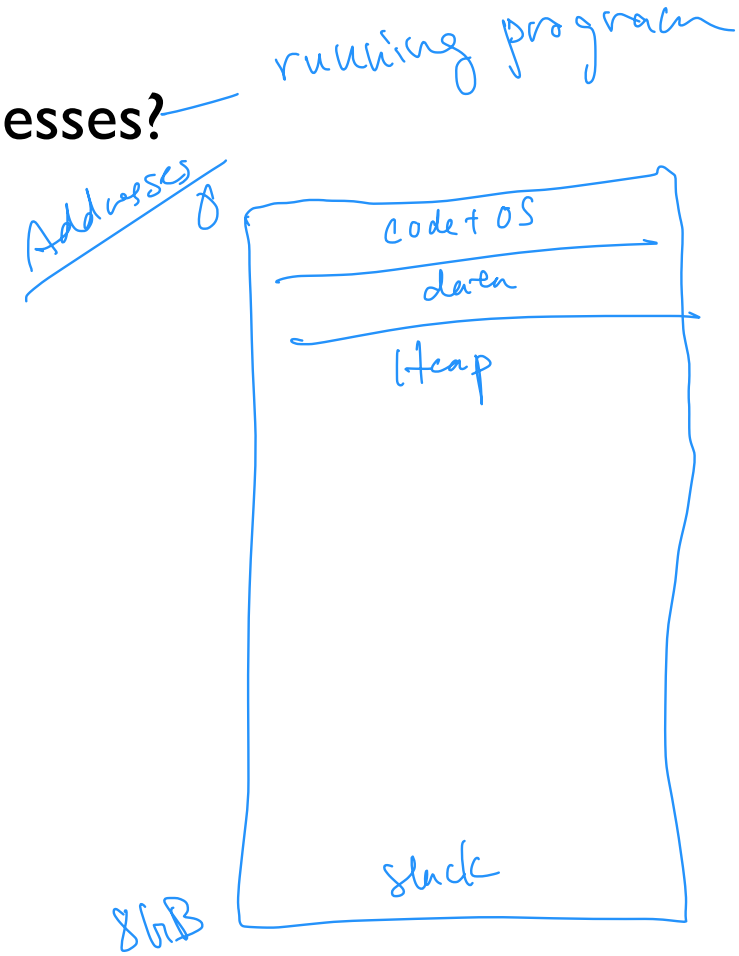
2^{60} = 1 EB

$2^{4} \times 2^{60} = 2^{64}$

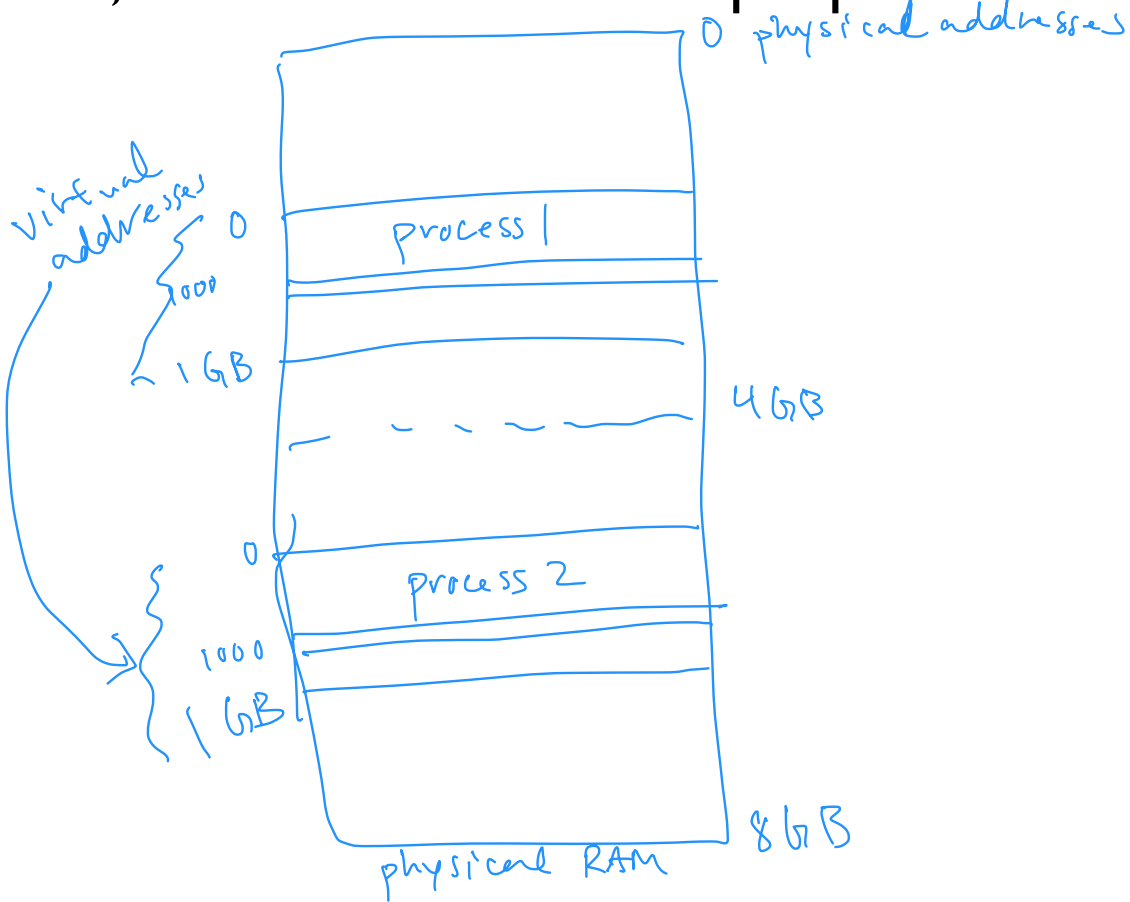
2^{4}: 16

2^{60}: EB

Remember processes?



With one RAM, how can we run multiple processes?



Memory virtualization

- Memory virtualization: divide up physical RAM into smaller "virtual" memory spaces
  - So each process thinks it has its own memory

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- Memory virtualization: divide up physical RAM into smaller "virtual" memory spaces
  - So each process thinks it has its own memory
  - The physical memory can be smaller than the ISA's address space
  - Hardware and software cooperatively manage how virtual memory maps to physical memory

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- Address generated by each instruction in a program is virtual address
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- Address translation maps virtual address to a physical address

