Lecture 19: Speculative execution

CMPE 120: Computer Organization & Architecture

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Logistics

- Reminder: check-in with professor is 1% of your final grade
  - Sign up link

- Midterm grades released last Friday

- HW4 out - start now if you haven't!!

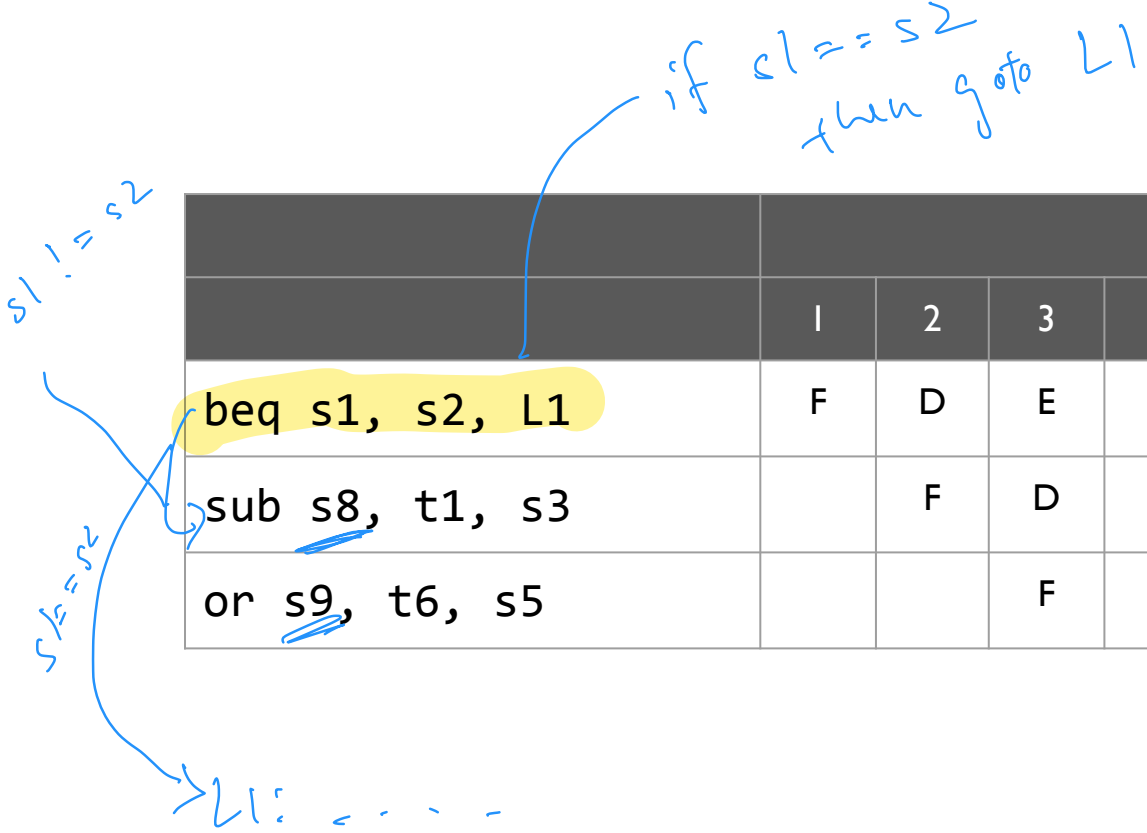
Reviewing mid-semester feedback survey

- 29 / 67 students responded (43% response rate)
  - Positives
    - Drawing on slides live
    - Interactive teaching with in-class participation using iClicker (even if iClicker finicky)
    - Being open to questions
    - Practice midterm exam
    - 1-on-1 meetings
  - Negatives
    - Grading scheme is stressful
    - Lecture pace is just right and too fast
    - More examples
    - Release practice final exam earlier
    - Hard to know how to tackle homework

Addressing the negatives

- Grading scheme is stressful
  - Considering several options for grade remediation
- Lecture pace is just right and too fast
  - Will try to slow down a little
- More examples
  - Will try to include more in slides
- Release practice final exam earlier
  - Will do. Aiming for 12/1
- Hard to know how to tackle homework
  - TAs will host homework discussion and work sessions during their office hours

Is there any issue here?



	Cycle							
	1	2	3	4	5	6	7	8
`beq s1, s2, L1`	F	D	E	M	W			
`sub s8, t1, s3`		F	D	E	M	W		
`or s9, t6, s5`			F	D	E	M	W	

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- Depends! If branch is not taken, then no. If branch taken, then yes!

Control hazard

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  - Instructions will continue to be fetched !
  - These 2 instructions must be flushed if branch is taken

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- Control hazard: next instruction not decided yet (caused by branch)

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…								
`L1: add s7, s3, s4`				F	D	E	M	W

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  - Stalling for every branch is expensive…
    - 15-25% of all instructions are branches

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How to handle control hazards?

- Idea: stall until branch is resolved
  - Stalling for every branch is expensive…
    - 15-25% of all instructions are branches
  - Especially if branch is not taken--could have kept pipeline full!

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resolve branch condition here!

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`bubble/nop`			D	E	M	W		
`sub s8, t1, s3`		F	F	D	E	M	W	
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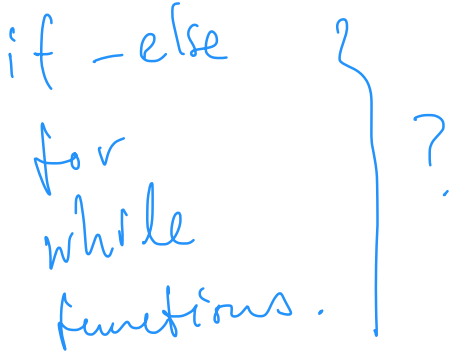


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Speculative execution

- The problem is that we must wait for branches to resolve

- But program behavior is predictable!
  - Examples?



Speculative execution

- The problem is that we must wait for branches to resolve

- But program behavior is predictable!
  - Loops
  - If statements checking for unlikely error conditions
  - Unconditional branches, i.e., jumps

```
int *arr = malloc(...)
if (arr == NULL)
    // if malloc failed
```

Speculative execution

- Idea: Processor makes educated guess if branch is taken or not
  - Known as speculative execution or branch prediction
  - Guess in Fetch stage--no more hazard!

- Two key questions:
  - How to guess?
  - What to do when guess is wrong?

Static Branch Prediction

- Simple idea: Always predict branch not taken
  - NextPC = PC + 4
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- What kind of program would this be bad for?

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- Simple idea: Always predict branch not taken
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- Performance (from CPI) depends on how accurate you are

- What kind of program would this be bad for?
  - Loop that's taken 95% of the time

How to predict branches?

- Static branch prediction
  - Predict always not taken
  - Predict always taken
  - Predict backward branches are taken, forward are not taken

~ 30-40 % accurate

~ 60-70 % accurate

How to predict branches?

- Static branch prediction
  - Predict always not taken
  - Predict always taken
  - Predict backward branches are taken, forward are not taken

- Pros:
  - Simple to implement

- Cons:
  - Poor accuracy

How to predict branches?

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  - Can we learn from the past and use it to predict the future?

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  - Can we learn from the past and use it to predict the future?

- Pros:
  - Prediction based on history can adapt to changes in branching behavior

- Cons:
  - More complex to implement (need additional hardware)

Dynamic branch prediction

history
0 → not taken
1 → taken

- 1-bit branch predictor: guess branch will take same direction as last time
  - Also known as last time predictor

history prediction

0 ⇒ not taken ⇒ uh-oh wrong! ⇒ update to taken ⇒ 1

1 ⇒ taken ⇒ uh-oh wrong! ⇒ update to not taken ⇒ 0

0 ⇒ not taken ⇒ right ⇒ stay same ⇒ 0
(update w/ same value)

1 ⇒ taken ⇒ right ⇒ stay same ⇒ 1

Dynamic branch prediction

- 1-bit branch predictor: guess branch will take same direction as last time
  - Also known as last time predictor
  - Ex: Last time branch was taken → Predict taken
  - Ex: Last time branch was not taken → Predict not taken

Dynamic branch prediction

- 1-bit branch predictor: guess branch will take same direction as last time
  - Also known as last time predictor

- Always mispredicts first and last iteration of loop branch $\frac{N-2}{N}$
  - What kind of loops will have high vs low accuracy?

loop w/ many iterations

loop that only has 1 iteration.

predict: N T N T

actual: T N T N

0% accuracy

What is needed to implement 1-bit branch predictor?

- We know the direction (taken vs not taken).

- We also need to know the…

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- Observation: Target address remains the same for conditional branches
  - Across dynamic instances

How to know where to jump to?

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  - Across dynamic instances

```
    addi s1, zero, 0    # s1 = sum
    addi s0, zero, 0    # s0 = i
    addi t0, zero, 10   # t0 = 10

For:                    # for (i = 0; i < 10; i += 1)
    bge  s0, t0, Done
    add  s1, s1, s0     # sum = sum + i
    addi s0, s0, 1      # i = i + 1
    j   For

Done:
```

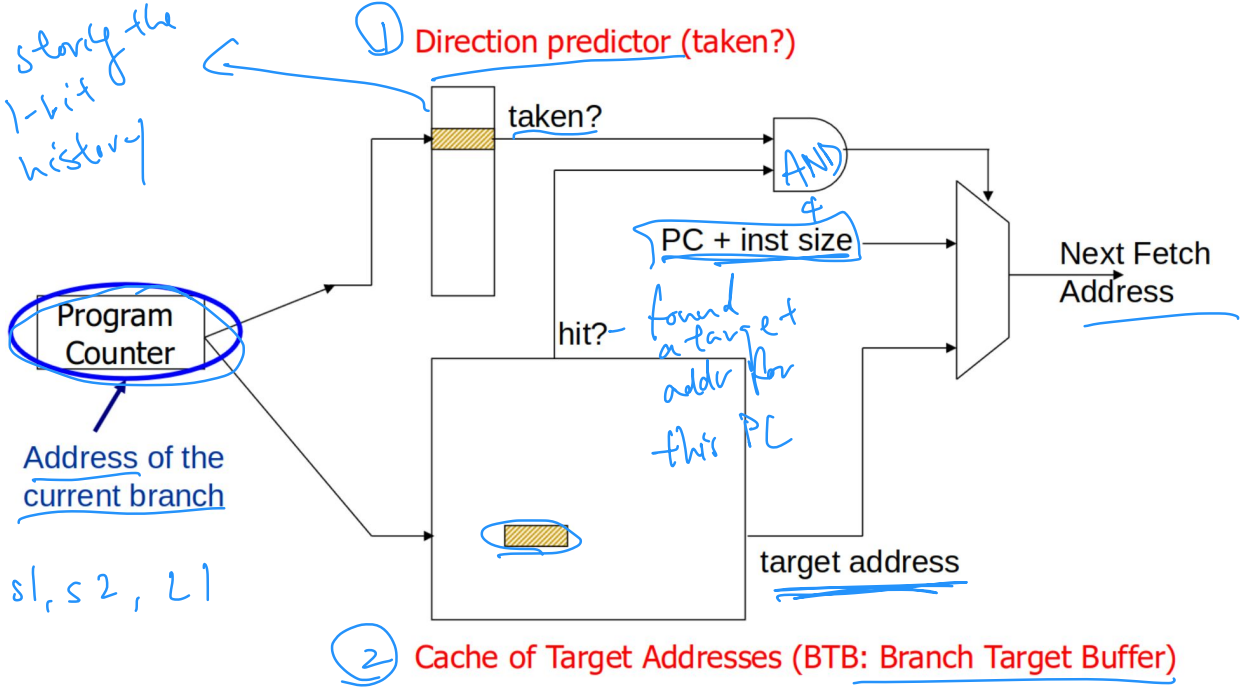
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- Idea: store target address from last time and access it with the PC
  - Called the Branch Target Buffer (BTB)

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Dynamic branch prediction

- 1-bit branch predictor
- 2-bit branch predictor
- Cache of target addresses (Branch target buffer)

What if I guess wrong?

- Branch condition not resolved until the Execute stage
  - These 2 instructions must be flushed if branch is taken
  - Known as flushing the pipeline

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- Branch misprediction penalty: # of instructions that must be flushed